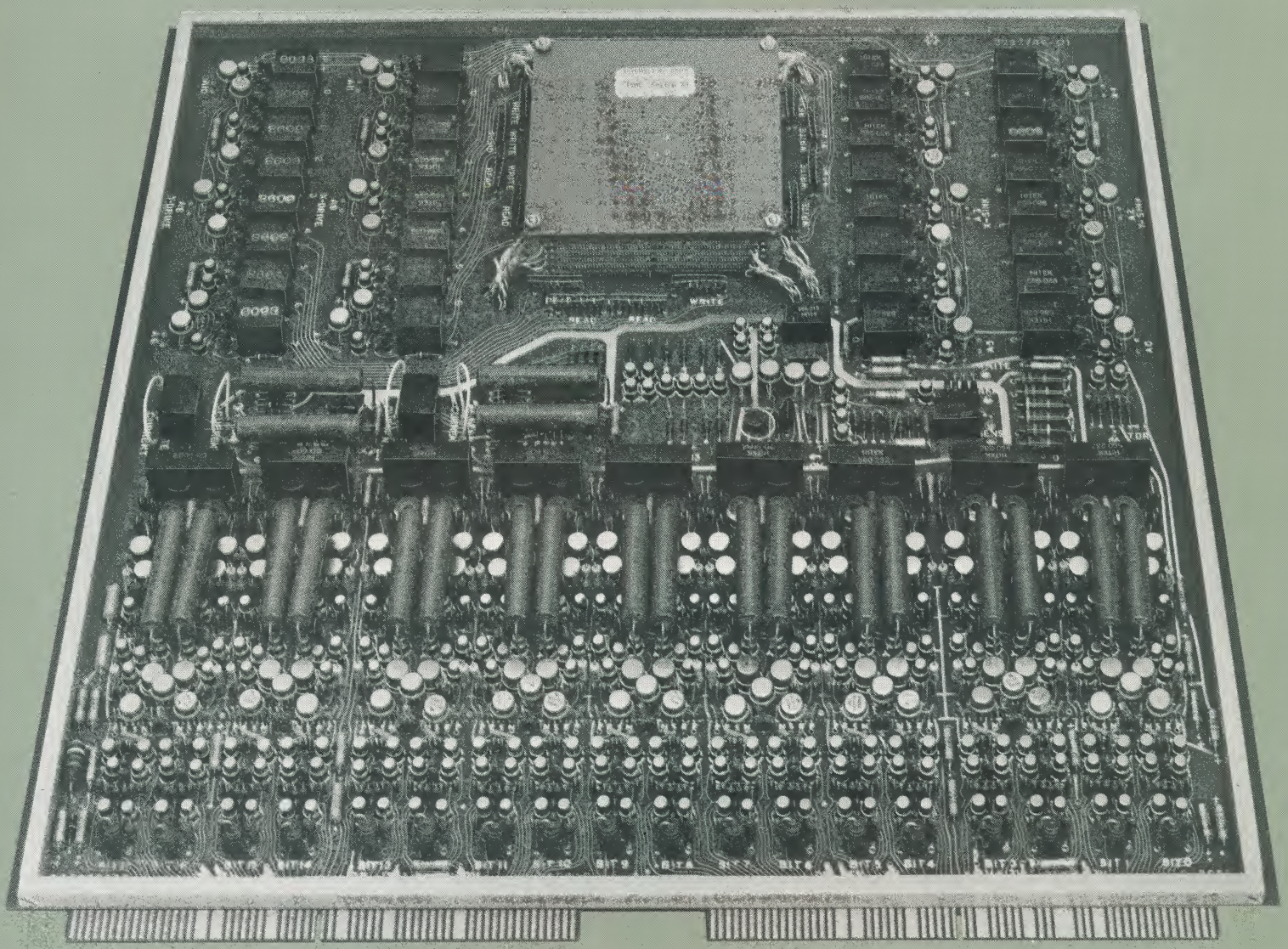
TYPICAL LARGE-SIZED PRINTED CIRCUIT BOARD ASSEMBLY USED IN RF FAMILY OF CORE MEMORIES.



AMPEX

RF

CORE MEMORIES

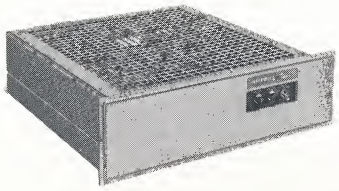
LOW COST FAMILY ▪ IMPROVED CONCEPT IN MEMORY SYSTEM PACKAGING ▪ ULTRA RELIABLE ▪ EXPANDABLE SYSTEMS ▪ WIDE RANGE OF INTERFACE LEVELS

RF

expandable, modular
core memory family

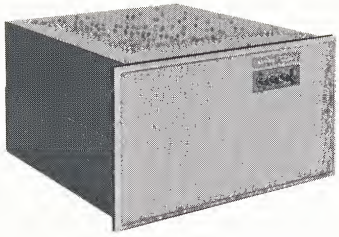
- **Large range of "store" sizes and options at moderate cost**
- **Capacities from 512 to 16,384 words in word lengths of 4 to 36 bits**
- **High MTBF . . . 5,000 hours for RF-1, proportional for RF-2 and RF-3**
- **Extreme memory compactness for all applications**
- **Simplified mechanical design includes "built-in" maintainability**
- **Nondestructive power shutdown**
- **1.8 microseconds full cycle time**
- **1.0 microsecond half-cycle time**
- **0.6 microsecond access time**

RF-1



- SMALL SIZED GENERAL STORAGE
- SMALL-TO-MEDIUM BUFFER APPLICATIONS
- SMALL SIZED COMPUTER "MAIN FRAME" APPLICATIONS

RF-2

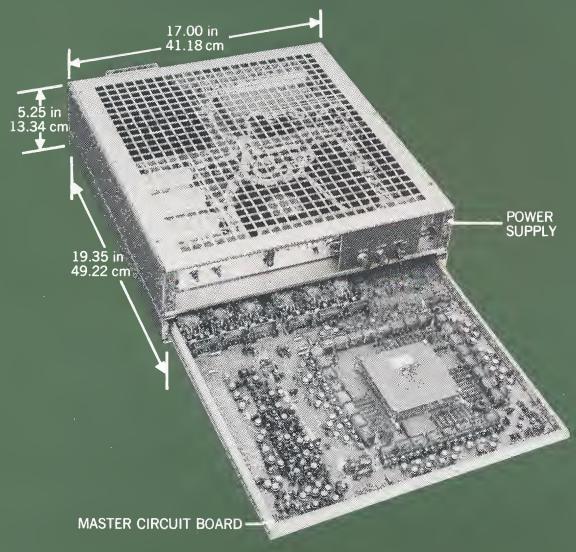


- SMALL-TO-MEDIUM SIZED GENERAL STORAGE AND BUFFER APPLICATIONS
- RANDOM AND SEQUENTIAL OR INTERLACED PROCESSING APPLICATIONS
- SMALL-TO-MEDIUM SIZED COMPUTER "MAIN FRAME" APPLICATIONS

RF-3

- MEDIUM-TO-LARGE SIZED GENERAL STORAGE AND BUFFER APPLICATIONS
- RANDOM AND SEQUENTIAL OR INTERLACED PROCESSING APPLICATIONS
- MEDIUM SIZED COMPUTER "MAIN FRAME" APPLICATIONS

RF CORE MEMORIES FIND USES IN: General Purpose Computing, Automatic Control, Digital Data Communication, A-D Conversion, Off-Line Data Processing, Media Conversion, Automatic Check-Out Equipment, Process Control, Machine Tool Control, Weapons Fire Control, Instrumentation, Multiplexing, Special Purpose Computing, Data Acquisition Systems.



RF-1

CAPACITY: 512, 1024, 2048 or 4096 words

WORD LENGTH: (in increments of 2 bits): 4 to 18 bits

MODES: Memory and Buffer

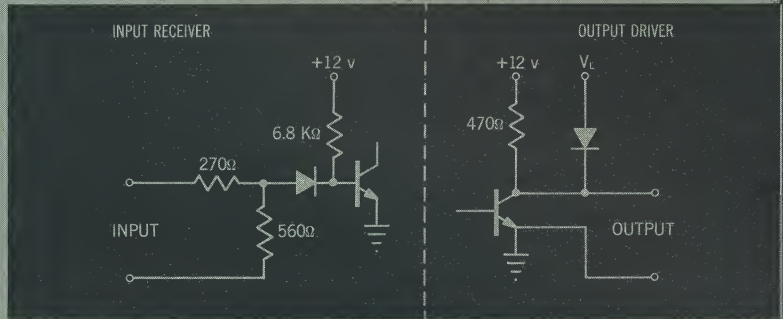
INPUT/OUTPUT:

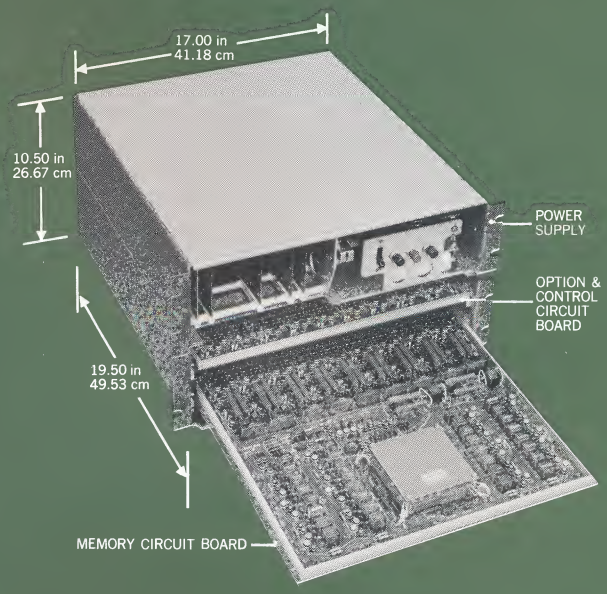
MAXIMUM INPUT IMPEDANCE: approx. 560 ohms

LOGIC CONVENTION: positive or negative

LOGIC STATES: +2 v, +4 v, +6 v and 0 v

TYPICAL INTERFACE CIRCUITS





RF-2

CAPACITY: 512, 1024, 2048, 4096 or 8192 words

WORD LENGTH: (in increments of 2 bits):

4096 words, 4–36 bits

8192 words, 4–18 bits

MODES: Memory and Buffer (with options)

INPUT/OUTPUT:

MAXIMUM INPUT IMPEDANCE: approx. 1800 ohms

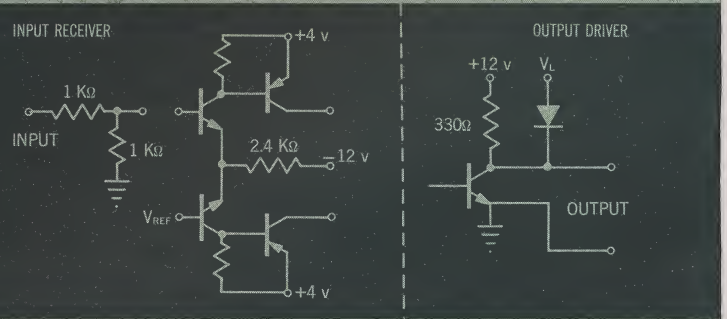
LOGIC CONVENTION: positive or negative

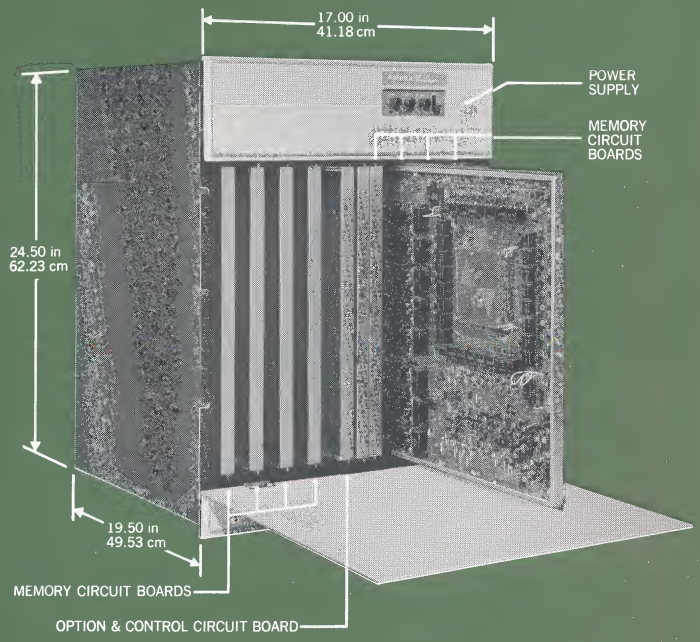
VOLTAGE POLARITY: positive or negative

LOGIC STATES: +2 v to +6 v, −2 v to −6 v and 0 v

MINIMUM THRESHOLD BAND: 1.1 v (centered between both logic levels)

TYPICAL INTERFACE CIRCUITS





RF-3

CAPACITY: 512, 1024, 2048, 4096, 8192, 12288 or 16384 words: (Larger capacity requirements can be satisfied by employing more than one memory.)

WORD LENGTH: (in increments of 2 bits):

4096 words, 37 to 72 bits
8192 words, 19 to 36 bits
12288 words, 4 to 36 bits
16384 words, 4 to 36 bits

MODES: Memory and Buffer (with options)

INPUT/OUTPUT:

MAXIMUM INPUT IMPEDANCE: approx. 1800 ohms

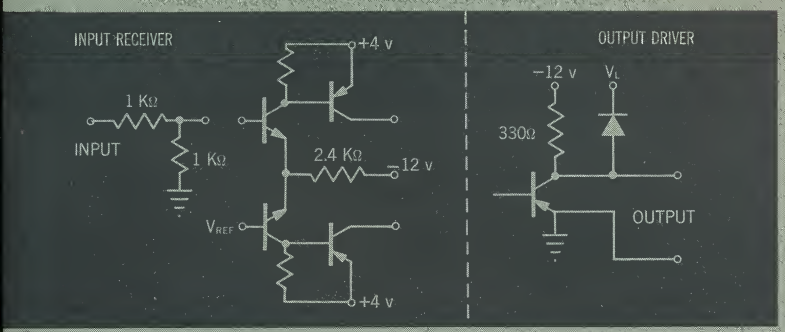
LOGIC CONVENTION: positive or negative

VOLTAGE POLARITY: positive or negative

LOGIC STATES: +2 v to +6 v, −2 v to −6 v and 0 v

MINIMUM THRESHOLD SWING: 1.1 v (centered between both logic levels)

TYPICAL INTERFACE CIRCUITS



Options

SEQUENTIAL AND SEQUENTIAL INTERLACE

This option permits the user to sequentially load or sequentially unload any group of addresses, or should he desire, the entire memory. Two Address Registers are provided so the load and unload operations can be "interlaced." During sequential operation of the memory, it is not necessary to present new address information prior to the initiation of each new cycle. The sequential operation may be started at any desired address by properly programming the memory. A "Random-Sequential" select line provides the user with a means for selecting the sequential mode of addressing or the standard random mode of addressing.

MASTER CLEAR

This option allows the user to clear all locations in memory and to reset all memory registers. The clear operation is accomplished by sequentially addressing all locations in memory and performing a "Read Only" operation on each location as it is addressed. The Master Clear operation is initiated by a pulse on the Master Clear Line and the time required for its execution is equal to: (number of memory locations + one) × (1 μsec.). The Memory Busy signal is in the "busy" state for the duration of the Master Clear operation. This option is only offered in conjunction with the "sequential" option.

ADDRESS REGISTER CLEAR

This option provides a means for resetting the Address Registers without disturbing the contents of the memory. A pulse on the "AR Clear" line will reset **both** Address Registers to the "all ones" state.

LAST ADDRESS

This option provides two output lines to the user to indicate when the "maximum count" address of the Load and/or Unload address registers has been selected. The Last Address signal is "true" during the cycle of the "maximum count" address and returns to a "false" level when the Address Register sequences to the next location — the all zero's address. This feature is useful in many applications as a buffer "full" or buffer "empty" indicator.

ZONE CONTROL

This option allows the user to segment the memory word (and therefore the memory register) into a maximum of four zones. By using the Zone Control lines in a Read-Modify-Write mode, the user can modify the selected segments (or zones) without altering the remaining zones of the Memory Register. No restriction is placed on bit arrangement per zone.

ADDRESS REGISTER OUTPUTS

This option provides the contents of the Address Register as single ended outputs from the Memory. Where two Address Registers are used, the "AR Outputs" represent the contents of the last address register employed — or the one currently being employed.

OPTIONAL INPUT POWER

The memory may be ordered for use with input power forms other than the 115 volt, 60 Hz domestic standard. These forms are defined in the General Specifications.

REMOTE POWER CONTROL

This feature provides the necessary lines to the user so DC power of the Memory power supply can be turned on and off from a remote location.

SELF CONTAINED MEMORY TESTER

A self contained tester is also offered as an option. The tester contains indicators for the address and data bits, a test pattern generator and automatic error checking circuitry. The tester provides the user with a means for "off-line" trouble-shooting of the memory.

General Specifications

Applicable to RF-1, RF-2 and RF-3 except as noted

TIMING:

Full Cycle, 1.8 microseconds

Half-Cycle, 1.0 microsecond

Access Time, 0.6 microsecond

OPERATIONAL MODES:

Clear-Write, Read-Restore, Write Only, Read Only, Read-Modify-Write

CONTROL SIGNALS:

Start Input Cycle (SIC), Start Output Cycle (SOC), Memory Buffer Select, Read-Modify-Write Select

OUTPUT SIGNALS:

Data Available, Memory Busy, End-of-Cycle, AC Failure

OPTIONAL SIGNALS (RF-2 and RF-3 only):

Random-Sequential Select, Master Clear, AR Clear, Zone Control Lines, Remote Power Control Lines, AR Output Lines, Last Address Output Lines

STANDARD INPUT POWER:

115 v ±10% of nominal, 60 Hz ±5%, single phase

OPTIONAL INPUT POWER:

115 v ±10% of nominal, 400 Hz ±5%, single phase

230 v ±10% of nominal, 50 Hz ±5%, single phase

APPROXIMATE INPUT POWER REQUIRED:

300 watts + 10 watts per bit

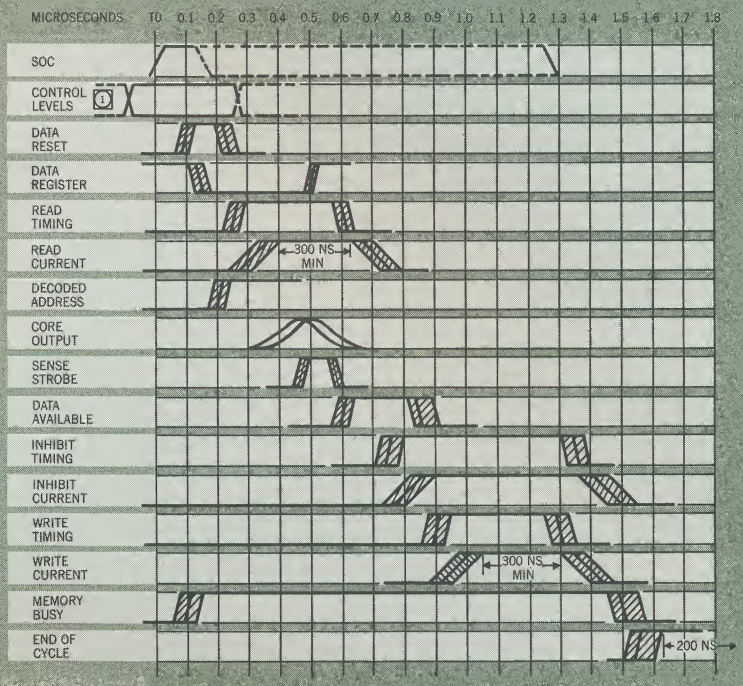
OPERATING ENVIRONMENT:

0° to 50°C (ambient), to 90% R.H. with no condensation

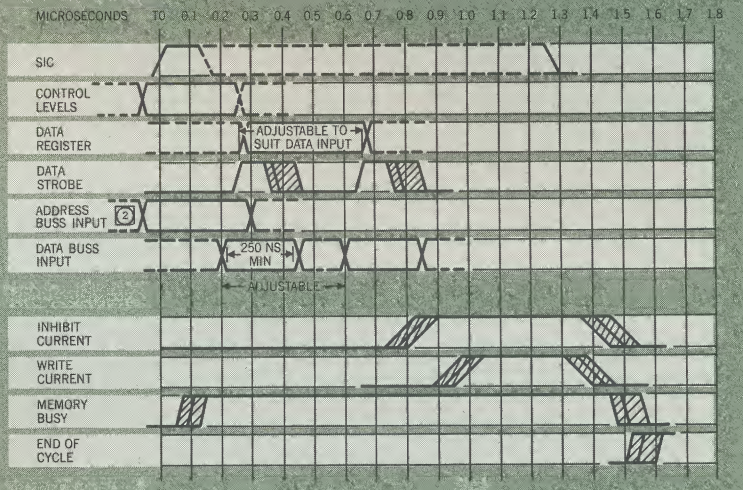
NON-OPERATING ENVIRONMENT:

−40° to +85°C, to 95% R.H. with no condensation; shock and vibration equivalent to conditions normally incurred during shipping

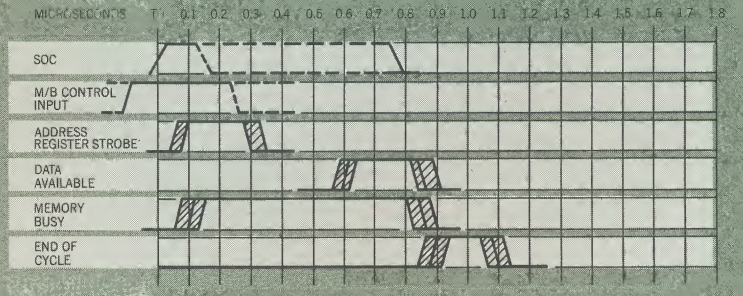
MEMORY MODE/READ-RESTORE



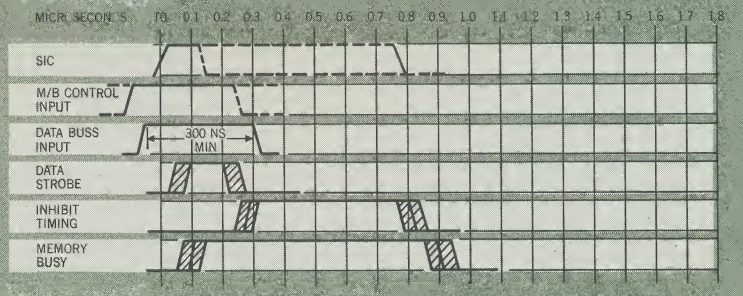
MEMORY MODE/CLEAR-WRITE



BUFFER MODE/READ ONLY



BUFFER MODE/WRITE ONLY



1 Control level inputs must be established 100 nanoseconds prior to T_o and must be sustained 250 nanoseconds after T_o. These levels need not return to zero between cycles.

2 Address inputs must be established 50 nanoseconds prior to T_o and must be sustained for 300 nanoseconds after T_o.

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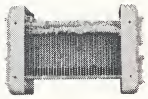
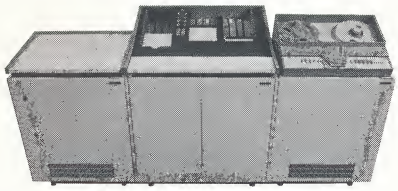
Ferrite Cores

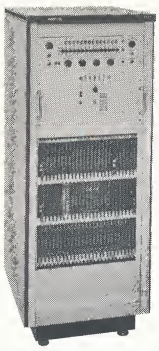
Core Memory Arrays



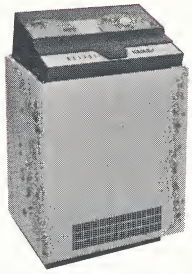
Core Memory Stacks



Data Conversion Systems

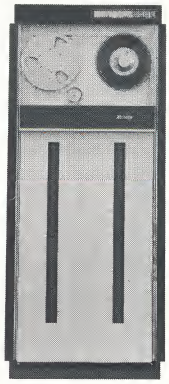


Core Memory Systems

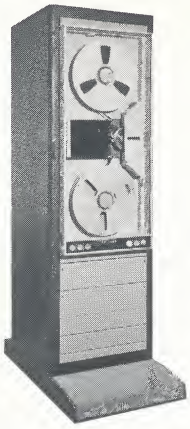


Moderate-speed Digital Tape Drives and Systems

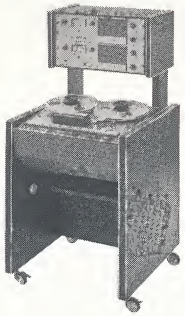
Document Storage and Retrieval Systems



High-speed Digital Tape Drives and Systems

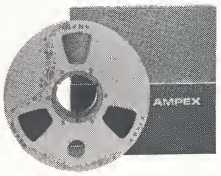


High-performance Instrumentation Recorders

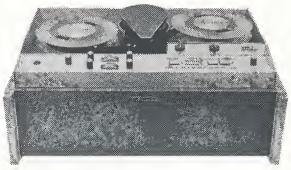


Professional, Educational and High-fidelity Audio Recorders

Superior Magnetic Tape for Computer, Instrumentation, Audio and Video Recording



Color Broadcast Videotape Recorders



Educational Closed-circuit and Home Videotape Recorders

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